WHAT IS CLAIMED IS:

1. A method comprising:

(a) using a phase-lock loop (PLL) to produce M clock phases from a reference signal;

(b) producing a count signal from the M clock phases;

(c) producing a shifted signal from the M clock phases and the count signal; and

(d) dividing the shifted signal to produce a feedback signal that is fed back to the PLL.

2. The method of claim 1, further comprising:

quantizing the count signal to produce a quantized signal, wherein the quantized signal in used to perform step (c).

3. The method of claim 2, wherein the quantizing step comprises using a truncator that outputs the most significant j bits of the count signal.

4. The method of claim 2, wherein the quantizing step comprises using a random number generator that adds one to or subtracts one from the count signal at a random time interval.

5. The method of claim 2, wherein the quantizing step comprises using a Sigma-Delta noise shaping method.

6. The method of claim 5, wherein the Sigma-Delta noise shaping method comprises using a noise shaping transfer function of $Z^{-1}/(1-Z^{-1})$.

7. The method of claim 1, wherein step (c) comprises using a a multiplexer (MUX) to perform the producing of the shifted signal.

8. The method of claim 1, wherein step (c) further comprises:

shifting the reference signal one phase every K/M cycles, wherein the reference signal is at least one of decreased by (K+1)/K and increased by K/(K-1).

9. The method of claim 1, wherein step (d) further comprises:

setting a frequency of the feedback signal using a divide-by-N element.

10. The method of claim 1, wherein step (b) further comprises:

extending a period T of the reference signal to at least one of T+T/M to perform frequency division of the reference signal and to T-T/M to perform frequency multiplication of the reference signal.

11. A method comprising:

(a) receiving a reference signal and a feedback signal at a clock generator;

(b) using the clock generator to generate M clock phases from at least one of the reference signal and the feedback signal;

(c) generating a count signal from the M clock phases;

(d) generating a shifted signal from the M clock phases and the count signal; and

(e) dividing the shifted signal to produce the feedback signal.

12. The method of claim 11, further comprising quantizing the count signal before it is used in step (d).

13. The method of claim 11, wherein step (d) comprises shifting the reference signal by one phase every K/M cycles.

14. The method of claim 11, wherein step (b) comprises using a phase-lock loop (PLL) as at least part of the clock generator.

15. The method of claim 11, wherein step (d) comprises using multiplexer (MUX) that receives the M clock phases at one terminal and the count signal at another terminal to generate the shifted signal.

16. The method of claim 11, wherein step (c) further comprises extending a period of the reference signal at least to T+T/M to perform frequency division of the reference signal and to T+T/M to perform frequency multiplication of the reference signal.